PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Wei CHEN, et al.

Docket No: Q57774

Appln. No.: 09/485,443

Group Art Unit: 2181

Confirmation No.: 1926

Examiner: KING, JUSTIN

Filed: May 1, 2000

For: METHOD OF OPTIMIZING THE TOPOLOGY OF THE IEEE 1394 SERIAL BUS

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of $500.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: February 22, 2005

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellants submit the following:

I. REAL PARTY IN INTEREST

The real party in interest is SAMSUNG ELECTRONICS CO., LTD, by virtue of an assignment executed by Chen Wei and Yun-Gik Lee (Appellants, hereafter), on March 15, 2000, and recorded by the Assignment Branch of the U.S. Patent and Trademark Office on August 18, 2000 (at Reel 011053, Frame 0801, Corrective Assignment to correct the spelling of the second Assignor's name recorded at Reel 010815, Frame 0164, on May 1, 2000).

II. RELATED APPEALS AND INTERFERENCES

To the knowledge and belief of Appellants, the Assignee, and the undersigned, there are no other appeals or interferences before the Board of Appeals and Interferences that will directly affect or be affected by the Board's decision in the instant Appeal.

III. STATUS OF CLAIMS

The application was originally filed with claims 1-5. Claims 1-5 are all of the claims currently pending in the application.

Claims 1-5 are rejected under 35 U.S.C. § 103 as being unpatentable over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

IV. STATUS OF AMENDMENTS

All amendments to the claims have been entered.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a method of optimizing the topology of a serial bus having a plurality of nodes, each of the nodes having one or more communication ports. According to one aspect of the invention, the nodes are prioritized according to the number of ports of the nodes and the transmission speed of the nodes. For example, in one embodiment the nodes shown in Figure 3A may be prioritized as shown in Figure 3B, with priority decreasing along the arrow connecting points A and B. (Page 4, lines 6-9.) In the example, the node to the far left of Figure 3B has a speed of 400 Mbps, followed by two nodes having speeds of 200 Mbps and three nodes having speeds of 100 Mbps. The three nodes having speeds of 100 Mbps are arranged in order of priority based upon the number of ports contained therein. Thus, the node having a speed of 100 Mbps and three ports has a priority higher than the node having a speed of 100 Mbps and two nodes.

An aspect of the invention also includes a step of connecting a non-used port of the node of the highest priority with a port of the node of the second next priority, and repeating the connecting step until all of the nodes are connected together, whereby the nodes are connected through the ports according to priority number. This results in a bus topology such as shown in Figure 3E. (Page 4, lines 10-17.)

According to another aspect of the invention, in certain situations, the priority of the nodes described above must be rearranged in order to accomplish a complete connection of all of the nodes. For example, prioritizing the nodes shown in Figure 4A according to the above-described technique results in the priority shown in Figure 4B. Connecting the nodes in the

manner described above results in a bus topology shown in Figure 4D in which there are no connections for two of the nodes. Accordingly, when all of the ports of the node of higher priority are used, the last connected node is separated and the node of the next priority is substituted for the last connected node. Thus, the priority is rearranged as shown in Figure 4E, and the resulting bus topology is shown in Figure 4F. (Page 4, line 21 to page 6, line 1.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-5 are rejected under 35 U.S.C. § 103 as being unpatentable over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

VII. ARGUMENTS

Claim 1 is not obvious over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

Claims 1 recites, *inter alia:*

> prioritizing said nodes according to the number of said communication ports and a transmission speed of said nodes, such that nodes of higher speed have higher priority than nodes of lower speed and nodes of equal speed are prioritized so that nodes having more of said communication ports have a higher priority than nodes having fewer of said communication ports.

Appellants respectfully submit that this feature is not taught or suggested by the references, taken either alone or in combination. The Examiner interprets section 8.4.6.2 of IEEE Standard for a High Performance Serial Bus as disclosing "that it is known to group nodes with the same speed capacity adjacent to one another because the high speed device's speed will be caped [sic, capped] by the lower speed parent device, and to reduce the number of hops." (Paper No. 14, numbered paragraph 3.)

First, there is no teaching whatsoever, explicit or implicit, or any suggestion, in section 8.4.6.2 to arrange nodes based on whether or not a device's speed will be capped. This section merely mentions that serial bus performance may be optimized by reconfiguring "the cable

topology in order to arrange nodes of the same speed capability adjacent to one another." (Underscoring added.) There is simply no support in section 8.4.6.2 for the Examiner's assertion that this section discloses "that it is known to group nodes with the same speed capacity adjacent to one another because the high speed device's speed will be capped by the lower speed parent device." (Underscoring added.) Appellants respectfully submit that this conclusion is impermissible hindsight gleened from the present application. Further, there is no teaching or suggestion in section 8.4.6.2 for the claimed feature of "prioritizing said nodes according to . . . a transmission speed of said nodes, such that nodes of higher speed have higher priority than nodes of lower speed" or of "connecting a non-used port of the node of the highest priority with a port of the node of the next priority." All that section 8.4.6.2 discloses or suggests is reconfiguring "the cable topology in order to arrange nodes of the same speed capability adjacent to one another." (Underscoring added.)

In the Advisory Action (Paper No. 16), the Examiner states:

> As Applicant states the standard does suggest arranging nodes of the same speed adjacent to one another; thus the standard suggests arranging nodes with same speed as the parent node and child node. Furthermore, since the child node's speed is capped by the parent node's speed when they have different speed capabilities, and each parent node can attach to several child nodes, a higher speed parent node is capable of supporting and optimizing several child nodes with several

> different speeds. Hence, the standard implicitly teaches the arrangement.

(Underscoring added.)

Appellants submit, however, that the underscored portion of the Examiner's comments are without support in the standard. There is simply no mention, explicit or implicit, of a child node's speed being capped by its parent, or of a higher speed parent being able to support and optimize several child nodes with several different speeds. The Examiner's reasoning seems to be an unwarranted expansion of the simple concept mentioned in the standard of reconfiguring "the cable topology in order to arrange nodes of the same speed capability adjacent to one another." (Underscoring added.)

In numbered paragraph 3 of Paper No. 14, the Examiner states:

> Douceur teaches that bandwidth reservation is known to guarantee resource (column 2, paragraphs 2-4). Since the isochronous transmission is a part of the 1394 features, the bandwidth reservation is a must practice; thus the nodes at the top of the 1394 tree will need higher bandwidth to support the isochronous transmission and to prevent speed capping. Hence it would have been obvious to one having ordinary skill in the computer art to combine Gorin and Douceur's teachings to implement the 1394's optimizing principles because they enable one to minimize the number of hops and to support the 1394 isochronous transmission.

Apparently, the Examiner's reasoning regarding the 1394 standard and Douceur is that the combination of these references teaches assigning a higher priority to higher speed nodes. (Appellants believe that the Examiner did not cite Gorin as teaching assigning a higher priority to high speed nodes, but cited Goring as teaching prioritizing so that nodes having more communication ports have a higher priority. The teachings of Gorin will be addressed below in the discussion of this aspect of the invention.)

As discussed above, section 8.4.6.2 of the 1394 standard does not teach or suggest prioritizing nodes according to the transmission speed of the nodes, such that nodes of higher speed have higher priority than nodes of lower speed. Douceur merely teaches bandwidth reservation. There is no teaching or suggestion that the bandwidth reservation is accomplished by prioritizing nodes based on speed or by connecting nodes based on priority. The Examiner's reasoning is hindsight based on Appellants' application. Appellants submit that section 8.4.6.2 of the 1394 standard and Douceur, as well as Gorin, fail to teach or suggest the claimed features of "prioritizing said nodes according to. . . a transmission speed of said nodes, such that nodes of higher speed have higher priority than nodes of lower speed" or of "connecting a non-used port of the node of the highest priority with a port of the node of the next priority."

In numbered paragraph 3 of Paper No. 14, the Examiner states:

> The implementation of reducing the number of hops for optimizing 1394 efficiency is beyond the IEEE standard's scope; however Gorin teaches that one of known implementation is to minimize the tree depth (column 6, lines 31-33) between the root and leaves; thus it

> implicitly teaches that it is known to place the nodes with higher number of ports at the top of the tree.

The Examiner cites Gorin as implicitly teaching that it is known to place the nodes with higher number of ports at the top of the tree. Appellants respectfully disagree with the Examiner's analysis that Gorin implicitly teaches placing the nodes with higher number of ports at the top of the tree.

First, as support for the proposition that Gorin implicitly teaches that it is known to place the nodes with higher number of ports at the top of the tree, the Examiner cites col. 6, lines 31-33, where Gorin mentions minimizing tree depth. But this portion of Gorin provides no teaching, explicit or implicit, for placing nodes with a higher number of ports at the top of the tree. At col. 6, lines 31-33, i.e., the section cited by the Examiner, Gorin teaches that "it is desired to create a binary tree having a minimum depth between the PE chosen as the root and the most remote leaf." This portion of Gorin describes an embodiment shown in Fig. 4 constituting a 4X4 array of 4-port PEs (col. 5, 60-64, and col. 6, lines 22-28). Fig. 4 illustrates the case where two PEs have faults, and it is desired to grow a tree using the functioning PEs in the array. (Col. 6, lines 28-31.) Although the tree grown is desired to have a minimum depth between the chosen root and the most remote leaf, there is no teaching or suggestion that "it is known to place the nodes with higher number of ports at the top of the tree", as asserted by the Examiner. Here, all the nodes have the same number of ports, that is four ports. So it does not follow that having a minimum depth between a chosen root and its most remote leaf in any way teaches or suggests placing the nodes with higher number of ports at the top of the tree.

Appellants submit that the IEEE 1394 standard, Douceur and Gorin, taken alone or in combination, do not teach or suggest:

> prioritizing said nodes according to the number of said communication ports and a transmission speed of said nodes, such that nodes of higher speed have higher priority than nodes of lower speed and nodes of equal speed are prioritized so that nodes having more of said communication ports have a higher priority than nodes having fewer of said communication ports;
>
> connecting a non-used port of the node of the highest priority with a port of the node of the next priority;

as recited in claim 1. At least for this reason, claim 1 is believed to be patentable over these references.

Claim 2 is not obvious over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

Moreover, dependent claim 2 is patentable at least because of its dependency from claim 1 and because the references fail to teach or suggest that "the step of prioritizing is performed so as to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports." In numbered paragraph 3 of Paper No. 14, the Examiner states; "since the 1394 node's speed will be capped by the parent node, the priority is assigned to the higher speed node to support the full performance of

the child nodes and the isochronous transmission." As discussed above, the 1394 standard does not teach or suggest anything regarding capping the speed of a parent node or assigning priority to a higher speed node. Additionally, this reference does not teach or suggest "to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports." The Examiner's analysis to the contrary is based on hindsight.

Claims 3 and 4 are not obvious over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

Claim 3, and its dependent claim 4, are believed to be patentable over the applied references for at least the reasons that claim 1 is patentable over these references. Claims 3 and 4 are also patentable for at least the following additional reason. Claim 3 recites, *inter alia:*

> separating the last connected node to assign to the node of the foremost priority among nodes in a next higher speed group than the separated last connected node when no port remains in the node of the lowest priority to connect with the node of next priority during the repeating step, whereby said nodes are connected through said communication ports according to priority order.

Appellants submit that this feature is not taught or suggested by any of the references, alone or in combination. Appellants note that the Examiner has not alleged that this feature is taught or suggested by the references.

Claim 5 is not obvious over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

Moreover, dependent claim 5 is patentable at least because of its dependency from claim 3 and because the references fail to teach or suggest that "the step of prioritizing is performed so as to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports." In numbered paragraph 3 of Paper No. 14, the Examiner states; "since the 1394 node's speed will be capped by the parent node, the priority is assigned to the higher speed node to support the full performance of the child nodes and the isochronous transmission." As discussed above, the 1394 standard does not teach or suggest anything regarding capping the speed of a parent node or assigning priority to a higher speed node. Additionally, this reference does not teach or suggest "to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports." The Examiner's analysis to the contrary is based on hindsight.

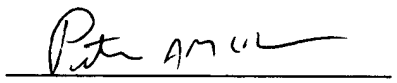
VIII. CONCLUSION

It is respectfully requested that the Board of Appeals and Interferences reverse the rejection of claims 1-5 as being unpatentable over the combination of "IEEE Standard for a High Performance Serial Bus", Gorin et al (U.S. Patent No. 5,020,059) and Douceur et al (U.S. Patent No. 6,247,061).

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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23373
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Date: February 22, 2005

APPENDIX

U.S. APP. NO. 09/485,443

CLAIMS 1-5 ON APPEAL:

1. A method of optimizing a topology of a serial bus having a plurality of nodes each with communication ports, comprising the steps of:

prioritizing said nodes according to the number of said communication ports and a transmission speed of said nodes, such that nodes of higher speed have higher priority than nodes of lower speed and nodes of equal speed are prioritized so that nodes having more of said communication ports have a higher priority than nodes having fewer of said communication ports;

connecting a non-used port of the node of the highest priority with a port of the node of the next priority; and

repeating the connecting step until all of said nodes are connected together, whereby said nodes are connected through said communication ports according to priority order.

2. A method as defined in Claim 1, wherein the step of prioritizing is performed so as to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports.

3. A method of optimizing a topology of a serial bus having a plurality of nodes each with communication ports, comprising the steps of:

comparing a total number of ports of all of said nodes with a reference value varying with the number (N) of said nodes to determine whether a prerequisite for constructing said topology

is satisfied, the prerequisite being that the total number of ports of all of said ports is not less than 2(N-1);

prioritizing said nodes according to the number of said communication ports and a transmission speed of said nodes when said prerequisite is satisfied, such that nodes of higher speed have higher priority than nodes of lower speed and nodes of equal speed are prioritized so that nodes having more of said communication ports have a higher priority than nodes having fewer of said communication ports;

connecting a non-used port of the node of the highest priority with a port of the node of a next higher priority;

repeating the connecting step until all of said nodes are connected together; and

separating the last connected node to assign to the node of the foremost priority among nodes in a next higher speed group than the separated last connected node when no port remains in the node of the lowest priority to connect with the node of next priority during the repeating step, whereby said nodes are connected through said communication ports according to priority order.

4. A method as defined in Claim 3, wherein the step of comparing determines that the prerequisite for constructing said topology is satisfied if the total port number of all of said nodes is equal to or greater than 2(N-1).

5. A method as defined in Claim 3, wherein the step of prioritizing is performed so as to firstly assign higher priority to the node of greater transmission speed, and then to secondly assign higher priority to the node having greater number of said ports.

EVIDENCE APPENDIX:

Pursuant to 37 C.F.R. § 41.37(c)(1)(ix), evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner and relied upon by Appellants in the appeal: NONE.

RELATED PROCEEDINGS APPENDIX

Copies of decisions rendered by a court or the Board in any proceeding identified about in Section II pursuant to 37 C.F.R. § 41.37(c)(1)(ii) submitted herewith: NONE.